Shared Test Hardware for Family IC

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Subject

- New test hardware development is time consuming and high cost. Normally the ICs are designed in series with similar package, distinct functions or vise versa.
- We can design and merge multiple ICs test into one test hardware at the beginning development.
- The merge and reuse of ATE test hardware for family IC will be introduced, the purpose is to elicit more ideas on test cost saving, test development time reduction.

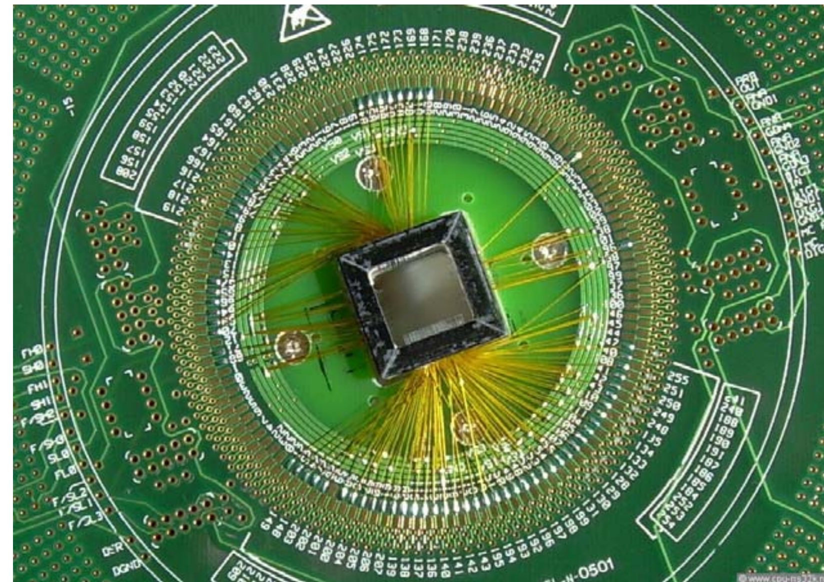
Outlines

Part 1	• ***Test Hardware Development Introduction***
Part 2	• ***Final Test Hardware Merge***
Part 3	• ***Probe Test Hardware Reuse***
Part 4	• ***Summary***

Part 1

- ***Test Hardware Development Introduction***

Handler Interface Board(HIB)



Probe Card(PC) + Probe Head(PH)

Test Hardware Development

- **When-** After system engineers have defined the product's technical requirements, design engineers developed the corresponding integrated circuit. Then test engineer generate hardware and software that will be used by ATE to guarantee the performance of each device after it is fabricated.
- **How long-** 2~4 months
- **Cost-** > $2K (PCB + components)

Current status-

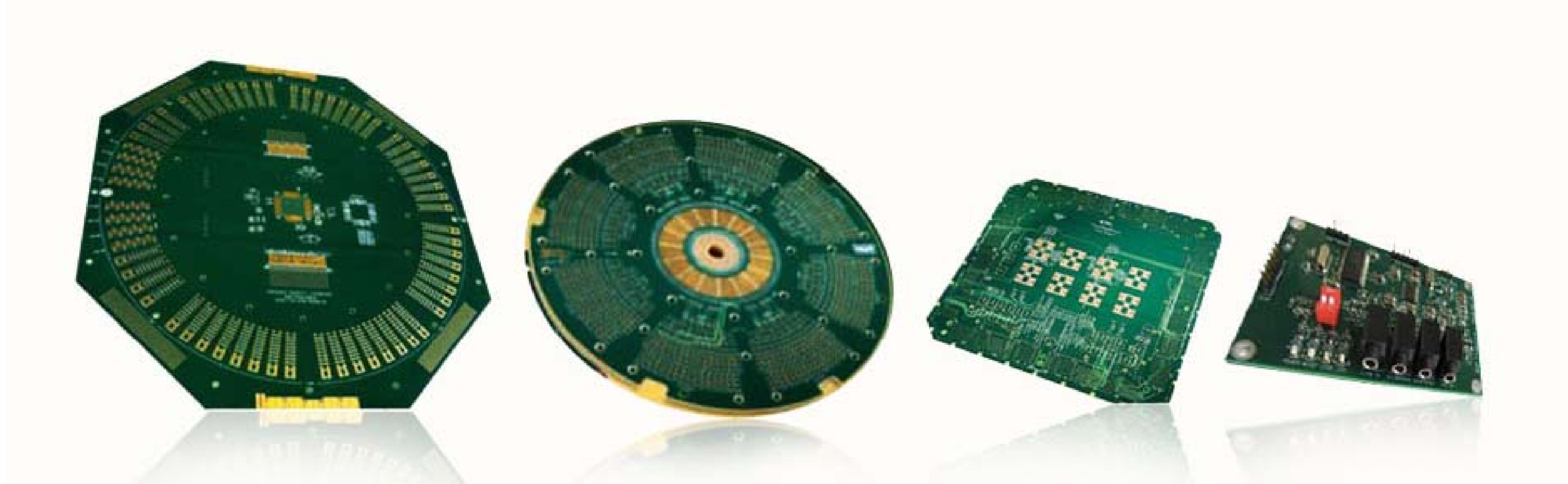
- Analog and mixed-signal DUTs usually require much more elaborate test hardware.
- Thus a test hardware is often intended for use with only one type of DUT mounted in a particular mechanical package.
- Clearly, electromechanical hardware design represents a large portion of the test engineering task.

Part 2

- ***Final Test HW Merge***

HIB Merge Description

- We usually have family ICs designed with distinct functions but in the same package, thus we can share HIB for them.
- The most commonly used HIB share is for adjustable output voltage/current ICs. For example, adjustable LDO.
- In DIB design we use relay to open/close different components for each IC. In test program, define different device names, like “LDO_1.5V”,”LDO_3.3V”, and select related test code.



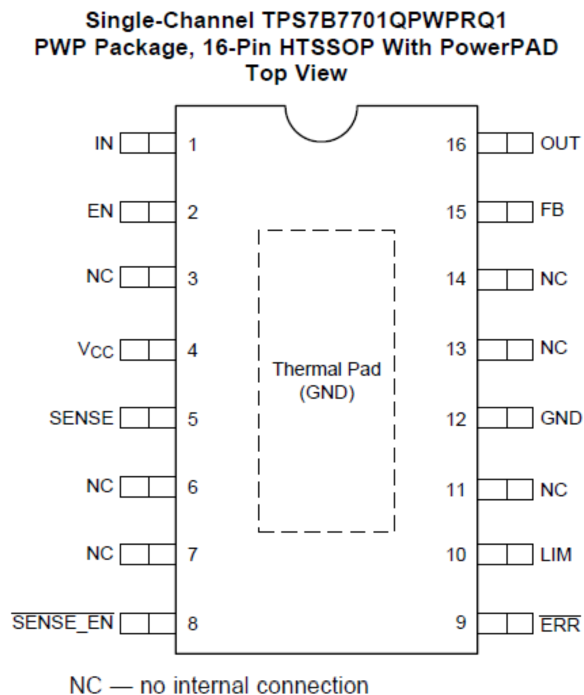
HIB Merge Example

Target device introduction:

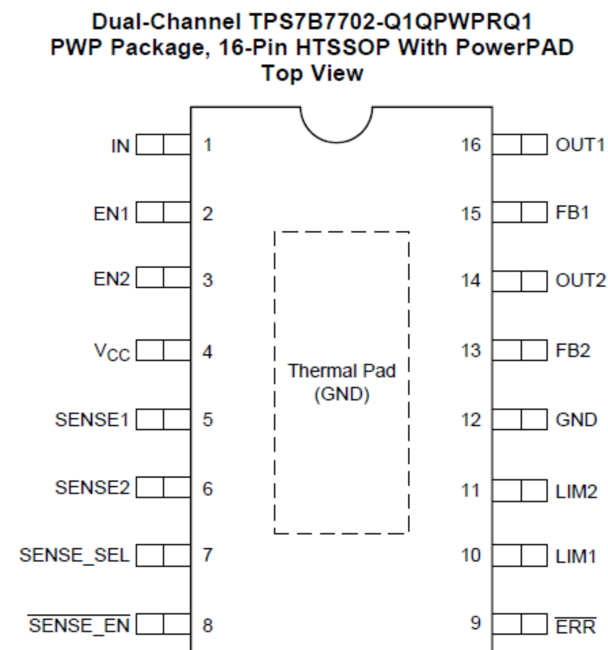
•TPS7B770x Single channel and Dual channel LED driver

•Same package HTSSOP-16

•Device introduction: Single/dual channel Antenna LDO with current sense.



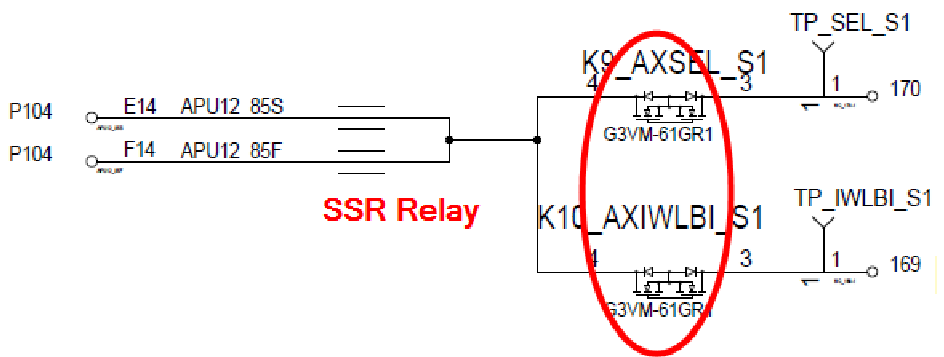
Single channel IC

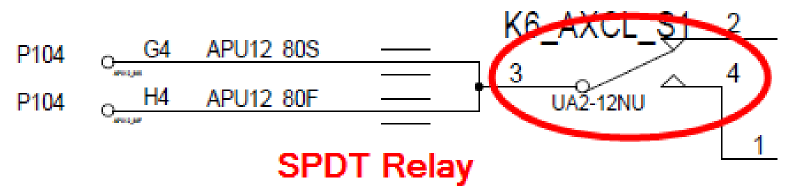


Dual channel IC

FT HW design process

HIB schematic design - Relay





Resource assignment for TPS7B770x

Reused pins	Resources	Extended pins	Resources
IN	fixed	EN 1/2	fixed
VCC	fixed	SENSE 1/2	fixed
SENSE_EN	fixed	FB 1/2	**Shared**
ERR	fixed	OUT 1/2	**Shared**

TI Automotive

HIB Merge Results

Benefit

- We can share test program, qualification boards…
- test hardware development time reduced 2~3 months
- cost saving $9K
- save load board check time during debug

Notics

- Earlier plan to collect more detail requirements for both ICs
- consider components space, ATE resources limitation since we merge two sets of test resources and need more relays
- Trade off between added test time and HIB cost if you need share much resources

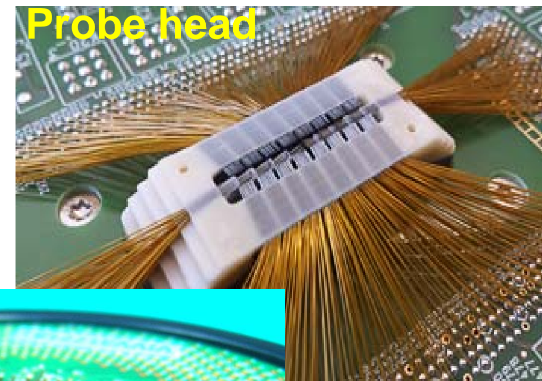
Part 3

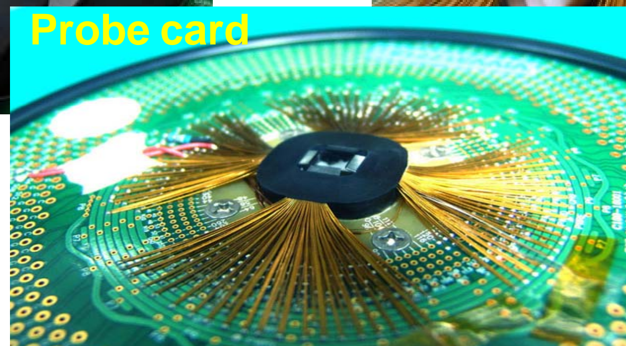
- ***Probe Test Hardware Reuse***

Probe Hardware Reuse Description

- Probe test is more elaborate, more specific thus very hard to reuse the whole test solution
- Probe test hardware includes three parts, very high cost

  Probe interface board(PIB) + probe card(PC) + probe head(PH)
- PC to PH connection need extra time
- We merge/reuse PC for multiple probe test





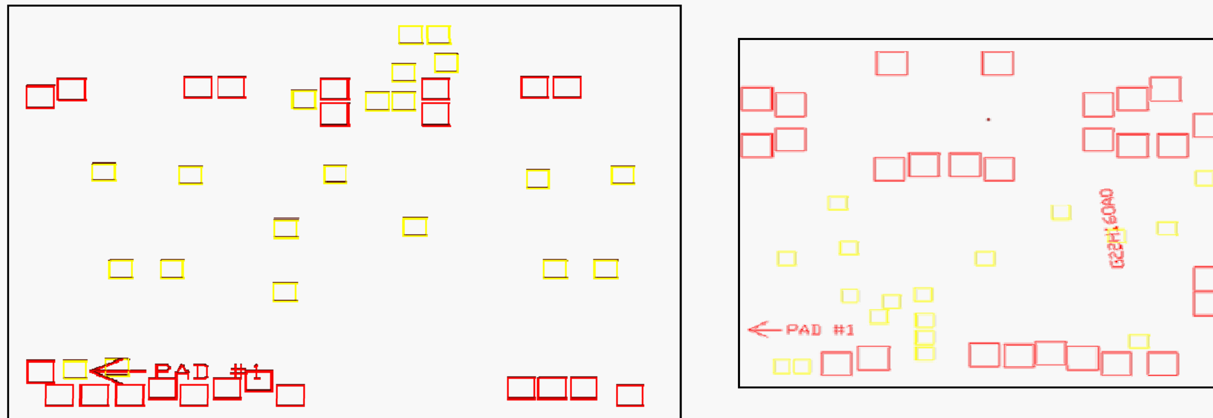
PC Reuse Example

Target device introduction:

•TPS4H160/000-Q1 Smart High Side Driver

•Die pad similarity: most pads are with same function, different pad numbers

•Device introduction: different Rdson(160mohm and 1ohm) QUAD channel high side drivers.



Different die pads for two ICs

PC Reuse Results

Benefit

- test hardware development time reduced 2~3 months
- cost saving $6K

Notice

- Move some components from PC to PIB can save the PC space

Part 4 • *Summary*

- Planning test HW design at the early phase of IC development
- Design more flexible universal test hardware – easy to reuse, sustaining, and high efficiency, they are very popular inside TI
- Except for test hardware, we can merge test program, manual test socket, and so on…

Q&A

Thank you!